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NETWORKED BASIC INPUT OUTPUT SYSTEM READ ONLY MEMORY

BACKGROUND

[0001] Many types of digital electronic machines (e.g., computers) include a local read only memory ("ROM") in which executable code is stored for use by the machine during an initialization process. The ROM and related circuitry may occupy an undesirable amount of space on a circuit board. Further, in systems having numerous computers coupled together in a network, managing the executable code stored in the ROMs of each computer can be problematic. For example, "flashing" the ROM (i.e., replacing some or all of the contents of the ROM) of each computer in a network having numerous computers can be an undesirably time-consuming and inefficient process.

BRIEF SUMMARY

[0002] In accordance with at least some embodiments of the invention, a system comprises a processor adapted to read BIOS code from a system ROM, a management controller coupled to said processor, and a network interface controller coupled to the management controller. The management controller selectively traps read accesses from the processor that target the system ROM and, in response, causes the network interface controller to load network BIOS code from storage external to the system during system initialization.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] For a detailed description of various embodiments of the invention, reference will now be made to the accompanying drawings in which:

[0004] Figure 1 shows a block diagram of a computer in accordance with various embodiments of the invention in which a management controller emulates a system ROM; and

[0005] Figure 2 provides a method implemented in the management controller of Figure 1.

NOTATION AND NOMENCLATURE

[0006] Certain terms are used throughout the following description and claims to refer to particular system components. As one skilled in the art will appreciate, various companies may refer to a component by different names. This document does not intend to distinguish between components that differ in name but not function. In the following discussion and in the claims, the terms "including" and "comprising" are used in an open-ended fashion, and thus should be interpreted to mean "including, but not limited to ...." Also, the term "couple" or "couples" is intended to mean either an indirect or direct electrical connection. Thus, if a first device couples to a second device, that connection may be through a direct electrical connection, or through an indirect electrical connection via other devices and connections.

DETAILED DESCRIPTION

[0007] The following discussion is directed to various embodiments of the invention. Although one or more of these embodiments may be preferred, the embodiments disclosed should not be interpreted, or otherwise used, as limiting the scope of the disclosure, including the claims. In addition, one skilled in the art will understand that the following description has broad application, and the discussion of any embodiment is meant only to be exemplary of that embodiment, and not intended to intimate that the scope of the disclosure, including the claims, is limited to that embodiment.

[0008] Referring now to Figure 1, a digital system 50 is shown in accordance with an embodiment of the invention. In the embodiment of Figure 1, the digital system 50 comprises a computer, but in other embodiments, the digital system may be other than a computer. As shown, computer system 50 comprises a processor 52 and system memory 54 such as random access memory ("RAM") coupled to a host controller 56. A pair of bridges 58 and 60 also couple to the host controller 56. The bridges 58, 60 provide connectivity to other devices in the system. Bridge 58 may couple to a network interface controller ("NIC") 62 and one or more other input/output devices 64 (e.g., keyboard, mouse, storage unit).

The NIC 62 may be coupled to an external network to permit the computer system 50 access to a network.

[0009] Bridge 60 may couple to a system ROM 66, management controller 70 and a second NIC 76 via a bus 65. The bus 65 may implement any suitable bus protocol such as the Low Pin Count ("LPC") protocol. The system ROM 66 may include executable code and data for use by the system 50. At least one such executable code is a local basic input/output system ("BIOS") 68. The local BIOS 68 comprises code that, when executed by the processor 52, facilitates the initialization of the system 50. The BIOS 68 also may provide code that permits the system to use various input/output device such as the NIC 62, a keyboard, a mouse, or a storage unit (collectively designated as the "other I/O devices" 64).

[0010] The system may initialize and operate using the local BIOS 68 contained in the system ROM. Alternatively and as explained below, the management controller 70 may permit the system to initialize and operate using a BIOS that is not contained within the system 50. For example, the network BIOS 92 stored in network storage 90 accessible to the system 50 via NIC 76 may be used instead of local BIOS 68. The management controller 70 may comprise a central processing unit ("CPU") 75 that executes code stored in ROM 72. Thus, some or all of the functionality attributed to the management controller 70 may be implemented by way of executable code executed by the controller's CPU.

[0011] In at least some embodiments, the management controller 70 may have its own power source (not specifically shown) that powers the management controller separately from the rest of the system 50. The separate power source may comprise a battery and/or an alternating current ("AC") power supply that provides a separately enabled source of power to the management controller 70. Having a separate power source permits the management controller 70 to be enabled and fully functional despite the rest of the system 50 being disabled and generally non-functional (e.g., powered "off").

[0012] The management controller 70 also couples to NIC 76. The NIC 76 may provide the system 50 with connectivity to a network that may be the same as or different from the network to which NIC 62 connects. The NIC 76 may be used to send and receive management control packets, while NIC 62 may be used to

send and receive data in accordance with applications that may run on system 50.

[0013] The management controller 70 may perform a variety of functions. At least one function implemented by the management controller 70 comprises, with the system 50 otherwise in an "off" state, interacting with the NIC 76 to determine when a management control packet is received into NIC 76 to request that the system transition to an "on" state. As such, an external management entity, such as a network manager 94, can remotely cause the system 50 to initialize.

[0014] Another function that may be implemented in the management controller 70 is to permit the system 50 to initialize without using local BIOS 68 and, instead, using network BIOS 92. This emulation capability of management controller 70 may permit the system 50 to avoid having a system ROM 66 at all, although the system ROM 66 can be included if desired. Network BIOS 92 may be the same or different as local BIOS 68. Being contained in network storage 90, network BIOS 92 can readily be edited and/or replaced by a network device such as network manager 94. Network manager 94 may comprise a computer system and be operated by a network administrator. The existence of the network BIOS 92 permits the network manager 94, or other network management entity, to manage the BIOS that is executed in system 50, and moreover, in additional BIOS-based systems, without having to interact with each such BIOS-based system separately to flash the various system ROMs 66. In accordance with an exemplary embodiment of the invention, the ability of the management controller 70 to cause the system to execute network BIOS 92 instead of local BIOS 68 involves maintaining the system ROM in a disabled state to prevent processor 52 from executing the local BIOS 68 and permitting the management controller 70 to emulate the operation of the system ROM 66 to load the network BIOS 92 in a way that is transparent to the processor 52. That is, processor 52 is generally unaware of whether the local BIOS 68 or the network BIOS 92 is being loaded and run in system 50.

[0015] Referring still to Figure 1, an optional logic gate 78 (which may comprise an "OR" gate or other suitable logic gate) receives two input signals and provides an output signal to the system ROM 66. One of the input signals to logic 78 is a

"reset" signal 79. The reset signal is asserted to a predetermined state during the initialization process when it is deemed acceptable for the system ROM 66 to begin functioning normally. In accordance with the embodiment of Figure 1, the reset signal is initially in the logic high state ("1"). The system ROM 66 is adapted to remain disabled while the reset signal is high. At an appropriate time during initialization (e.g., after the system's power supply has stabilized), the reset signal is caused to transition by reset circuitry (not shown) to the logic low state ("0") thereby causing the system ROM to transition from a disabled state to an enabled state. The logic state 78 is included to permit the network BIOS 92 to be run in system 50 or is not included to permit the local BIOS 68 to run in the system 50.

[0016] Output signal 83 from management controller 70 is provided as an input signal 81 to OR gate 78 and controls the output signal of the OR gate. Even when the reset signal transitions to a low state, the management controller 79 maintains the system ROM 66 in a reset mode to "emulate" the operation of the system ROM to permit the system 50 to initialize using the network BIOS 90. As noted above, the emulation performed by the management controller 70 generally is transparent to the rest of the system 50. That is, the system 50 may not be aware that the BIOS being executed is network BIOS 92 from an external storage 90 instead of local BIOS 68 system from system ROM 66.

[0017] The management controller 70 may be programmed to drive logic 1 on output signal 83 to permit the system 50 to initialize using the network BIOS 92, or may be programmed to drive logic 0 on output signal 83 to permit the system 50 to initialize using the local BIOS 68.

[0018] As noted above, the signal on the management controller's input 83 causes the management controller 70 to operate in one of a plurality of modes. In accordance with the embodiment of Figure 1, a first mode may be specified if the management controller 70 is programmed to drive output signal 83 to be a logic 1. In the first mode, the management controller 70 emulates the system ROM 66 to cause the network BIOS 92, not the local BIOS 68, to be executed by the system's processor 52. A second mode may be specified if the management controller 70 is programmed to drive output signal 83 to be a logic 0. In the second mode, the management controller 70 may not emulate the system ROM

66 thereby permitting the system's processor 52 to execute local BIOS 68, instead of network BIOS 92.

[0019] The first mode (in which the management controller 70 emulates the system ROM 66) will now be described with reference to Figures 1 and 2. During initialization of system 50, the management controller 70 is programmed to determine whether the management controller should emulate the system ROM 66 (decision block 202). If the management controller 70 determines that emulation mode is not being specified, then, as indicated by block 204, the management controller enters the second mode that may comprise a non-emulate mode in which the management controller performs any one or more of a variety of other functions (e.g., send and receive management control packets via NIC 76).

[0020] If, however, the management controller 70 determines that the first mode is being specified, then control passes to block 206 in which the system management controller "traps" accesses to the system ROM 66. Trapping an access refers to detecting when an entity, such as processor 52, initiates a transaction that targets the system ROM. The system ROM 66 may reside in a memory map at a predetermined address that also is known to the management controller. As such, the management controller 70 monitors bus 65 for transactions that include the address corresponding to the system ROM 66. During the first mode of operation, the system ROM 66 is disabled as described above and thus the system ROM 66 is unable to respond to any transactions targeting the system ROM. Instead, the management controller 70, having detected a transaction targeting the system ROM 66, responds to the transaction as if the management controller 70 was the system ROM 66. In this way, the processor 52 need not be aware of whether the system ROM 66 or the management controller 70 has responded.

[0021] The transaction initiated by the processor 52 to the system ROM 66 may comprise a read access by which the processor 52 requests the system ROM to provide one or more instructions for execution by the processor. In the first mode of operation, the management controller 70 causes the requested instructions to be retrieved from the network storage's network BIOS 92 (block 208). In general,

the requested instructions are provided from the network storage 90 and through NIC 76, bridge 60 and host controller 56 to the processor 52.

[0022] A number of variations on how to provide the network BIOS 92 to the processor are possible. For example, in some embodiments when the management controller 70 receives the first read request for local BIOS 66 from the processor 70, the management controller 70 may respond by signaling the network storage 90 to begin providing the entire network BIOS 92 to the management controller. Thus, the management controller 70 effectively requests, not only the specific instructions being requested by the processor, but also some or all of the remaining instructions in the network BIOS in anticipation of future read requests from the processor for such instructions. Upon retrieval, the network BIOS 92 may be stored in the management controller's RAM 74 pending retrieval by the processor 52. In other embodiments, the management controller 70 requests the network storage 90 to provide only the instructions being requested by the processor 52.

[0023] The management controller 70 may need to know or otherwise determine the location of the network BIOS 92 in the network storage device 90. In some embodiments, the management controller 70 may be programmed a priori with the beginning address of the network BIOS 92. Of course, a change to the location of the network BIOS 92 will necessitate a change to management controller's programming to reflect such a change. In other embodiments, the management controller 70 requests the network BIOS 92 location from a suitable network entity such as the network manager 94. The network manager 94 responds to the management controller 70 with the starting location of the network BIOS 92 thereby permitting the management controller to begin retrieving the network BIOS 92.

[0024] The management controller 70 also may need to know the size of the network BIOS 92 to ensure that the management controller retrieves the entire network BIOS. The size information may be programmed into the management controller 70 or may be provided to the management controller via the network manager 94.

[0025] Once the management controller 70 has retrieved one or more instructions from the network BIOS 92, such instructions may be provided to the requesting processor 52 for execution therein (block 210). As explained above, the processor 52 may not be aware that the instructions originated from the network BIOS.

[0026] In some embodiments, the system ROM 66 is installed in the system 50, but disabled as explained above. In other embodiments, the system ROM is not installed in the system 50, but the management controller 70 is configured to emulate the system ROM so that the processor 52 need not be aware of the absence of the system ROM. In this latter embodiment, board space is saved due to the absence of the system ROM 66.

[0027] The above discussion is meant to be illustrative of the principles and various embodiments of the present invention. Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.